REMARKS

This Amendment is in response to an Office action dated 12/3/2002. A response is due 03/03/2003, and can be extended. A request for extension of time is included herewith.

This application was filed as a continuation of commonly-owned, copending U.S. Patent Application No. 09/166,499 filed 10/05/98 (now USP 6,279,045, issued 8/21/01). The Examiner is the same (Chun Cao).

Claims 23-46 are pending in the application, including the following independent claims:

23, 29, 30, 31, 33, 35 and 37, all directed to multimedia interface,

38, 39, 40, 42, 44 and 46, all directed to signal processing interface.

Double Patenting

The Examiner rejects all of the claims based on non-statutory double patenting.
This rejection is overcome by the filing of a "Terminal Disclaimer" (enclosed herewith)

35 USC 102 and 103

Claims 23, 26-28, 31, 33, 35, 42 and 44 are rejected under 35 USC 102 (e) as being anticipated by Martel (USP 5,887,165). Specifics are set forth in the Office action.

Claims 23-24, 26-29, 31-36, 38 and 40-45 are rejected under 35 USC 102 (e) as being anticipated by Gilson (USP 5,600,845). Specifics are set forth in the Office action.

Claims 24-28, 30 and 39 are rejected under 35 USC 103 (a) as being unpatentable over Gilson, in view of Chang (USP 5,687,325). Specifics are set forth in the Office action. We note that Chang was cited in the parent case.

Allowable Subject Matter

The Examiner has noted that **Claims 37 and 46** are allowable over the prior art.

Amendments to the Claims

Arguments Traversing the Rejection

A. Claim 23 and 47

a. Martel (USP 5,887,165)

Martel discloses a dynamically reconfigurable hardware system for real-time control of an external device. (ABSTRACT)

In a preferred embodiment of the reconfigurable hardware system 11 shown in Fig. 1 will be manufactured as part of an expansion card to be plugged into a PCI expansion slot. (col. 3, lines 38-59) There is no indication that the components, i.e., a filed programmable gate array 13, a random access memory 15, a processor 17, a configuration memory 19, and a dedicated I/O port 31, on the card 11 are incorporated on a same IC chip. Specifically, although Martel states that the processor 17 and the random access memory 15 may be implemented as a single digital signal processor 21, Martel does not indicate that any other components may be implemented with the processor 17 as a single IC chip.

Therefore, Martel does not teach or suggest a multimedia interface comprising a block of reconfigurable logic and a media processor incorporated on a same IC chip.

Claim **47** further recites a configuration port. See page 12, lines 6-9 of the specification (A configuration port 106 allows a user access to the reconfigurable logic 102 from off-chip).

In Martel, programming the field programmable gate array 13 is achieved by sending a configuration signal from a controller (processor 17). In response to the configuration signal, the gate array's internal gates are set according to the contents of the configuration memory 19. That is, the processor 17 (or the DSP 21) coordinate and control the programming of the gate array 13. (col. 5, lines 4-19, col. 2, lines 12-16, claim 1)

Of course, the field programmable gate array 13, as a stand-alone IC separate from the processor 17 and the configuration memory 19, has a configuration port (the port connected to the configuration memory 19). If the components on the card 11 were incorporated on a same IC chip, however, such one-chip IC would not have the configuration port. That is, the configuration in the configuration memory block would be provided to the field programmable gate array block through an internal connection between these two blocks.

b. Gilson (USP 5,600,845)

Gilson discloses an integrated circuit computing device comprised of a dynamically configurable field programmable gate array (FPGA). The gate array is configured to implement a RISC processor and a reconfigurable instruction execution unit. (ABSTRACT)

The RISC processor 14 is coupled to Programmable Memory 42 which contains the code (instruction). (col. 5, lines 32-34)

However, Gilson does not teach or suggest that the instruction of the RISC processor 14 includes a virtual instruction set capable of implementing a variety of multimedia algorithms. Compare **claims 23 and 53**.

On the contrary, Gilson clearly explains that a RISC (Reduced Instruction Set Computer) processor only has a simple instruction set, as opposed to a CISC (Complex Instruction Set Computer) which are high power, complex, general purpose microprocessor that would allow the execution of complex instruction. Specifically, Gilson states, "The RISC architecture concentrated on implementing each instruction within a simple instruction set in a single clock cycle. The underlying philosophy of the RISC architecture is to do fewer functions than the CISC architecture, but to do them very fast. As a result of the reduced, simplified instruction set, the amount of circuitry in a RISC is substantially less than used in a CISC. So for a RISC machine, there is no MULTIPLY instruction. The MULTIPLY operation would be accomplished in a RISC machine by a software routing performing series of ADD and SHIFT instructions". (col. 1, line 49 - col. 2, line 5)

B. Claims 29 and 38

Each of amended claims 29 and 38 corresponds to one of the selections of allowable **claim 37 or 46**. Therefore, claims 29 and 38 should be allowable.

C. Claims 48 and 54

Each of added claims **48** and **54** recites audio and/or video CODEC and an analog

interface incorporated on the IC chip, the audio and/or video CODEC communicating, via the analog interface, with external analog signals.

See page 12, lines 19-24 (the media processor 104 can communicate, via an analog interface 100, with off-chip multimedia signal sources) and page 14, lines 1-3 (communicating over lines 180 and 182, respectively, with external signal sources) of the specification.

Gilson does not teach or suggest this feature.

Gilson discloses an expansion board 60 including a FPGA 12 and an audio input portion 69, which includes a Dual 18-bit A/D Converter 90. However, the A/D Converter 90 is implemented separately from the FPGA 12, which is an IC chip in which the RISC Processor 14 is incorporated. (Fig. 3, col. 8, lines 1-25)

There is no indication that the RISC Processor 14 and the A/D Converter 90 may be incorporated on a same IC chip.

Chang (USP 5,687,325) discloses a graphic controller 60 that may include a compressed image CODEC 74. If the CODEC 74 operates as a decoder, it receives compressed digital data and converts such data into uncompressed digital video data (Fig. 2, col. 7, lines 6-15). If the CODEC 74 operates as an encoder, it receives uncompressed digital video data and converts such data into compressed digital video data. In either case, the CODEC 74 does not receive analog signal. Therefore, the graphic controller 60 does not have an analog interface.

Even if the computing device 10 of Gilson were modified to incorporate the CODEC 74 of Chang on the same IC chip, the computing device 10 still would not have an analog interface.

D. Claims 30, 39 and 49, 55

Each of amended claims 30 and 39 corresponds to one of the selections of allowable claim 37 or 46. Therefore, claims 30 and 39 should be allowable.

Added claims **49** and **55** are means-plus-function form claims corresponding to amended claims 30 and 39. Therefore, claims **49** and **55** should be allowable.

E. Claims 31, 40 and 50 and 56

Each of amended claims 31 and 40 corresponds to one of the selections of allowable claim 37 or 46.

Added claims **50** and **56** clarifies that the serial interface standard is one of USB and IEEE-1394.

Therefore, claims 31 and 40 (and dependent claims **50** and **56**) should be allowable.

F. Claims 32, 41 and 51 and 57

Each of amended **claims 32 and 41** recites a programmable, fast serial interface core to interface to a serial interface standard incorporated within the reconfigurable logic block.

a. Martel (USP 5,887,165)

Martel does not teach or suggest the feature of **claim 32 or 41**.

As already explained, Martel does not teach or suggest a multimedia interface comprising blocks of reconfigurable logic and a media processor incorporated on a same IC chip. Therefore, although the reconfigurable hardware system 11 of Martel manufactured as part of an expansion card has an I/O port 31, Martel does not teach or suggest a multimedia interface comprising blocks of reconfigurable logic, a media processor, and a programmable, fast serial interface core all incorporated on a same IC chip, as in **claim 32**. Similarly, Martel does not teach or suggest a signal processing interface comprising blocks of reconfigurable logic, a RISC core, and a programmable, fast serial interface core all incorporated on a same IC chip, as in **claim 41**.

Further, Martel shows, in Fig. 1, the I/O port 31 separately from the FPGA 13. There is no indication that the I/O port 31 may be incorporated within the reconfigurable logic block

(FPGA 13).

b. Gilson (USP 5,600,845)

The serial interface core according to the claimed invention allows the user to interface to various serial interface standards such as USB, IEEE-1394 or other serial link. (page 14, line 29 - page 15, line 1 of the specification). Although not disclosed in this application, the serial interface core controls, in order to interface to a particular interface standard, the exchange of data in accordance with a data exchange protocol determined for the particular interface standard. To this purpose, the serial interface core includes circuitry such as a serial interface engine 206, 312, 412 as disclosed in the commonly-owned application 09/166,501 (US Patent 6,370,603).

Gilson does not teach or suggest a serial interface core to interface to a serial interface standard incorporated on the IC chip.

Gilson discloses a computing device 10 implemented in a FPAG, such as Xilix XC3000, which comprises I/O Blocks 32. (col. 5, lines 40-49) However, there is no indication that the I/O Blocks 32 functions as a serial interface core to interface to a serial interface standard.

In fact, Gilson does not disclose any external device that communicates to the computing device 10 or the FPGA 12 with a serial interface standard. Further, Gilson does not teach or suggest that the I/O Block 32 includes a serial interface engine or other circuitry necessary to interface to a serial interface standard.

c. Gilson in view of Chang

Chang does not teach or suggest a serial interface core incorporated within the reconfigurable logic block.

Chang discloses an ASIC System Logic Controller (SLC) 10 having a bus interface 26 that permits the SLC 10 to exchange data with a bus included in a digital computer system such as ISA, EISA, VESA, PCI, VME. The SLC 10 may included two different bus interfaces 26, one with interfaces a PCI bus, and another which interfaces an ISA, an EISA, or a SCSI bus.

However, none of the buses disclosed in Chang is a serial bus.

ISA is an 8-bit parallel bus. EISA and VESA are 32-bit parallel buses PCI is a 32 or 64-

bit parallel bus. VME is a 16 or 32-bit parallel bus. SCSI is an 8 or 16-bit parallel bus.

Further, Chang incorporates the bus interface 26 as one of fixed functional units separately from the FPGA 48. (col. 3, lines 21-37) Therefore, the bus interface 26 is not incorporated within the reconfigurable logic block (FPGA 48).

G. Claims 33 and 42

Each of amended claims 33 and 42 corresponds to one of the selections of allowable claim 37 or 46. Therefore, claims 33 and 42 should be allowable.

H. Claims 35 (and 36) and 44 (and 45)

Each of amended claims 35 and 44 recites a programmable memory interface (PMI) core incorporated on the IC chip, the PMI core communicates with off-chip memory and configures it virtually into what is optimal for an application that demands non-standard size memory.

See page 14, lines 10-24 of the specification.

None of the cited references teach or suggest this feature.

I. Claims 52 and 58 (and 36 and 45)

Each of added claims **52** and **58** corresponds to one of the selections of allowable claim 37 or 46. Therefore, claims **52** and **58** should be allowable.

Supplemental Information Disclosure Statement

A Supplemental Information Disclosure Statement was filed, April 18, with the following references.

USP 5,301,278	USP 5,307,320	USP 5,623,234	USP 5,663,687
USP 5,734,913	USP 5,737,746	USP 5,815,725	USP 5,835,435
USP 5,842,029	USP 5,860,016	USP 5,864,704	USP 5,949,484
USP 5,977,997	USP 6,021,500	USP 6,035,349	USP 6,061,794
USP 6,119,194	USP 6,122,747	USP 6,131,125	USP 6,425,054

Newly-Presented Claims
Claim Count

Claims 47-58 (twelve total) are newly-presented herewith, of which claims 48, 49, 52, 54, 55, 58 are in independent form.

The highest number of claims previously paid for is:

24 total claims (4 excess)
13 independent claims (10 excess)

After entry of this Amendment, there will be
36 total claims (numbered 23-58)
19 independent claims

thereby necessitating fees for

12 excess total @ $ 18	$ 216
6 excess independent @ $84	$ 504

Conclusion

The claims should be allowed.

Various fees are enclosed herewith.

For the Applicant

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